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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,514	11/03/2003	Fu-Chia Shone	MR2707-48	1385
4586	7590	10/26/2004	EXAMINER	
ROSENBERG, KLEIN & LEE 3458 ELLICOTT CENTER DRIVE-SUITE 101 ELLICOTT CITY, MD 21043			HO, TU TU V	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/698,514	Applicant(s) SHONE, FU-CHIA	
	Examiner Tu-Tu Ho	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 11/03/2003 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention I, claims 1-17, and cancellation of claims 18-23 in the reply filed on 09/27/2004 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- 3 **Claims 1-17** are rejected under 35 U.S.C. 102(e) as being anticipated by Harari et al.

U.S. Patent Application Publication 2003/0109093.

Harari discloses in Figures 1-12 and respective portions of the specification a common spacer dual gate memory cell as claimed.

Referring to **claim 1**, Harari discloses a common spacer dual gate memory cell comprising:

two bit lines (also labeled as S/D, 152 and 153, Figs. 7-9, or 186 and 187, Figs. 10-12, and paragraph [0061] for the disclosure that S/D is also bit line) on a semiconductor substrate (163 or 183, Figs. 7-9 or Figs. 10-12 respectively);

a first channel (no number) for a first transistor and a second channel (no number) for a second transistor arranged in series between said two bit lines;

a first gate dielectric (165 or 201, Figs. 7-9 or Figs. 10-12 respectively) and a second gate dielectric (also labeled 165 in Figs. 8-9, or 203 in Figs. 11-12, respectively) above said first and second channels, respectively;

a first control gate (157 or 192, Figs. 8-9 or Figs. 11-12 respectively) and a second control gate (160 or 198', Figs. 8-9 or Figs. 11-12 respectively) above said first and second gate dielectrics, respectively; and

a spacer (167 or 203, Figs. 8-9 or Figs. 11-12 respectively) between said first and second control gates;

wherein at least one of said first (165 or 201) and second (165 or 203) gate dielectrics includes a silicon nitride (paragraph [0064] and note that the characteristics of gate dielectric 107 ("charge storage dielectric layer") described in paragraph [0064] apply to gate dielectrics 165 and 201).

Regarding **claim 2**, the Harari's memory cell inherently comprises a punch through region between the two bit lines, which as noted above also act as S/D regions, where "punch through region" is interpreted literally as a region that punch through is likely to occur. For proof of inherency, see for example U.S. Patent 6,566,699 to Eitan et al., which, in disclosing a memory cell having a gate dielectric 18/20/22 including a silicon nitride and a control gate 24,

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teaches in columns 11 and 14, particularly column 14, lines 25-35, how a punch through region is formed in the region between S/D regions 14 and 16.

Referring to **claim 3**, Harari further discloses that said first control gate extends along a first direction and said second control gate extends along a second direction perpendicular to said first direction (best seen in Figs. 7-8A and Figs. 10-11A).

Referring to **claim 4**, Harari further discloses that said second control gate (160 or 198', Fig. 8A or Fig. 11A respectively) has a portion crossing over above and isolated from said first control gate (157 or 192).

Referring to **claim 5**, Harari further discloses that said spacer (167 or 203) is formed on a sidewall of said first control gate (157 or 192, best seen in Fig. 8A and Fig. 11A).

Referring to **claim 6**, Harari further discloses that said spacer and first control gate extend along a same direction (best seen in Fig. 8A and Fig. 11A).

Referring to **claim 7**, Harari further discloses that said second control gate has a portion crossing over above said spacer (best seen in Fig. 8A and Fig. 11A).

Referring to **claim 8**, Harari further discloses that said second control gate (160 or 198') has a portion in a trench to contact said second gate dielectric (165 or 203, best seen in Fig. 8A and Fig. 11A).

Referring to **claim 9**, Harari further discloses that said first and second gate dielectrics (165 and also 165, Figs. 8-9) each comprises a silicon nitride (as noted above).

Referring to **claims 10 and 11**, Harari further discloses that one of said two transistors is completely turned on during the other one is read and that one of said two transistors is completely turned on during the other one is programmed (paragraphs [0072] through [0082],

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particularly paragraph [0072], "One segment of the cell is turned on hard, thus eliminating any effect of its programmed threshold level, while the other is being programmed or read").

Referring to **claim 12**, Harari further discloses that one (203, Figs. 11-12) of said first (201) and second (203) gate dielectrics includes an oxide only (paragraph [0103]).

Referring to **claims 13 and 14**, Harari further discloses that said oxide gated transistor is turned on during the other one is programmed and that said oxide gated transistor is turned on during the other one is read (paragraph [0107]).

Referring to **claim 15**, Harari further discloses that silicon nitride gated transistor is programmed with two charge storage locations (171 and 172, Fig. 9, paragraphs [0069] through [0071], particularly the last passage of paragraph [0071]).

Referring to **claim 16**, Harari further discloses that said two charge storage locations are programmed with a threshold voltage substantially different from each other (paragraphs [0085] through [0089], particularly the middle passage of paragraph [0089]).

Referring to **claim 17**, Harari further discloses that silicon nitride gated transistor is programmed with one charge storage location (171) next to said spacer (paragraph [0069]).

4 **Claims 1 and 2** are rejected under 35 U.S.C. 102(e) as being anticipated by Sasago et al. U.S. Patent 6,670,671.

Sasago discloses in Figure 2A and respective portions of the specification a common spacer dual gate memory cell as claimed.

Referring to **claim 1**, Sasago discloses a common spacer dual gate memory cell comprising:

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two bit lines (205, “source lines”, “data lines” or “bit lines”, column 7, first paragraph and column 14, first paragraph) on a semiconductor substrate (200);

a first channel (no number) for a first transistor and a second channel (no number) for a second transistor arranged in series between said two bit lines;

a first gate dielectric (202) and a second gate dielectric (210) above said first and second channels, respectively (note that gate dielectric is interpreted as a dielectric for a gate and “above” is interpreted broadly);

a first control gate (207a, “third gate”, column 7, lines 24-30: “the third gate 207a functions as the gate for controlling the channel under the third gate 207a”) and a second control gate (211a) above said first and second gate dielectrics, respectively; and

a spacer (such as 206a or 208a) between said first and second control gates;

wherein at least one of said first and second (210) gate dielectrics includes a silicon nitride (column 9, lines 23-26).

Regarding **claim 2**, Sasago further discloses a punch through region (501) between said two bit lines (205, where “punch through region” is interpreted as a doped region for preventing punch-through between S/D regions).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tu-Tu Ho
October 21, 2004